Page 1, line 4, please insert the following new headings and paragraph:

## CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE99/03881 which was published in the German language on November 30, 1999.

## TECHNICAL FIELD OF THE INVENTION

Page 1, line 10, please insert the following new heading:

## BACKGROUND OF THE INVENTION

Page 1 please replace the paragraph beginning on line 11 with the following rewritten paragraph:

According to EP 0 198 684 B1, a differential relay operates to protect an electric power transmission line which is monitored at various points with regard to the current flowing through. The currents at the various points on the power transmission line are converted into digital input signals by using a dedicated operating clock in each case to sample the power supply line to be monitored at the various points. The sampling is undertaken in this case at the various points not with the aid of a synchronous clock, but with the aid of weakly differing clock frequencies. Running between the various points of the power supply line is a digital transmission channel via which a calling message is transmitted by a detecting device (master) at one point of the power supply line to another point, the calling message also including data which give information on the sampling instant at the one point. In response to the calling message, a detecting device (slave) at the other point of the power supply line emits a return signal which includes, inter alia, the information on the sampling instant in the master and on a time difference between the last sampling instant in the slave and the subsequent receiving instant of the calling message in the slave. The return signal received by the master is used in the master to draw a conclusion on the temporal skew of the sampling instants at the two different

points on the power supply line, and the time skew is compensated with regard to the various sampling instants after a vector transformation of the received data by means of an appropriate pointer rotation.

Page 2, line 9, please insert the following new headings and paragraphs:

## SUMMARY OF THE INVENTION

In an embodiment of the invention, a plurality of digital input signals, formed by sampling with dedicated operating clock in each case forms digital auxiliary signals by sampling the digital input signals with a common postprocessing clock, which is at least twice as fast as the fastest operating clock. The digital input signals form synchronized digital output signals which correspond to the digital input signals by interpolating each digital auxiliary signal.

In one aspect of the invention, sampling the common postprocessing clock, filtering the digital input signals with a filter which is an inverse of a characteristic of an interpolation filter used for interpolating.

In another aspect of the invention, filtering an antialiasing filter directly after the interpolation occurs.

In a further aspect of the invention, the digital input signals are obtained from secondary variables, sampled with a dedicated operating clock, of measuring transducers in an electric power supply system.

In yet a further aspect of the invention, digital input signals are formed from secondary variables of Rogovsky measuring transducers, the digital auxiliary signals are formed directly from the input signals, and an integrator is used for the interpolation.

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 illustrates an exemplary embodiment of an arrangement for carrying out the method according to the invention.

Figure 2 shows an exemplary embodiment of a filter for filtering the digital input variables.

Figure 3 shows the characteristic and structure of the filter according to Figure 2.

Figure 4 illustrates an exemplary embodiment of an interpolation filter.

Figure 5 shows the characteristic and structure of the filter according to Figure 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Page 2, please replace the consecutive paragraphs beginning on line 10 and ending on page 4, line 20 with the following rewritten paragraphs:

The invention is a method for synchronizing a plurality of digital input signals such that it can be carried out relatively easily and reliably without the need to form pointer variables.

According to the invention, digital auxiliary signals are formed by sampling the digital input signals with the aid of a common post-processing clock. Use is made of a post-processing clock which is at least twice as fast as the slowest operating clock. Synchronized digital output signals which correspond to the digital input signals are formed by means of interpolating each digital auxiliary signal.

An advantage of the method according to the invention is that it can be used to synchronize a plurality of digital input signals even when these input signals are formed from analog input signals by sampling with the aid in each case of a very different operating clock. Consequently, the clock generators required for generating the operating clocks need to fulfil only relatively low requirements for the purpose of carrying out the method according to the

invention. Moreover, the method according to the invention places relatively modest requirements on the quality of the transmission channels. A further advantage is that the method according to the invention can be carried out relatively easily, because the sampling of digital input signals with the aid of a common post-processing clock, and the interpolation of the digital auxiliary variables thus formed are well-established measures.

The method according to the invention can be carried out with sufficient accuracy when the digital input variables are sinusoidal and/or cosinusoidal signals. When sinusoidal and/or cosinusoidal signals are not used, errors may occur. If the error is not acceptable with regard to the given requirements, it may be advantageous to, before being sampled with the aid of the common post-processing clock, filter the digital input signals with the aid of a filter having a characteristic which is the inverse of the characteristic of an interpolation filter used for the interpolation. In this embodiment, a transmission characteristic with the value 1 results on the transmission link of the digital input variables up to the formation of the digital output variables, resulting in the possibility of forming digital output variables which correspond very perfectly to the digital input variables.

It is advantageous to apply filtering with the aid of an anti-aliasing filter is undertaken directly after the interpolation, in order to achieve a bandwidth limitation for an evaluation device to which the digital output signals are to be applied.

The digital input signals to be synchronized can be of different formation. For example, they can be output signals of sensors which respectively use individual clock generators to output digital signals at their output from analog input variables. Furthermore, the digital input signals can be generated from analog measured variables of an electric power supply system by sampling at various points on the power supply system. The method according to the invention is

also advantageous when the digital input variables are obtained from secondary variables, sampled with the aid in each case of a dedicated operating clock, of measuring transducers in an electric power supply system. In this case, the measuring transducers can be arranged at various positions, for example in a transformer substation, or can be obtained as a component of a differential protective arrangement at the ends of an electric power supply line or at other terminals of a generator or power transformer.

Page 4, please replace the consecutive paragraphs beginning on line 29 and ending on page 7, line 21:

As illustrated in Figure 1, an analog input signal x(t) at input, is converted in an analog-to-digital converter 2 into a digital input signal x(k). This digital input signal x(k) traverses a signal encoder 3 formed by a differentiator, resulting at the output of the signal encoder 3 in a pulse train xd(k) which has been produced by differentiating the digital input signal x(k). A transmission device 4 transmits the pulse train xd(k) via a transmission channel 5 to a receiving device 6 which outputs the pulse train xd(k) on the output side.

The arrangement illustrated in Figure 1 includes a receiving device 7 which is connected with its input 8 to an input 9 of the arrangement similar to the receiving device 6 with reference to the input 8. The dotted illustration is intended to include an analog-to-digital converter corresponding to the analog-to-digital converter 2, a signal encoder corresponding to the signal encoder 3, a transmitting device corresponding to the transmitting device 4, and a transmission channel corresponding to the transmission channel 5. A pulse train yd(k) obtained in accordance with the pulse train xd(k) of the signal y(t) is then produced at the output of the further receiving device 7.

In addition to the receiving device 7, it is also possible for additional receiving devices to have additional pulse trains applied to them in the same way.

On the output side, a signal decoder 10, which includes a resampling device 11 on the input side, is connected to the receiving devices 6 and 7. This resampling device 11 can be designed and operated as illustrated in detail in US patent 5,075,880, particularly in Figure 5, and described in conjunction therewith. Thus, in the resampling device 11, the digital input signals xd(k) and yd(k) are respectively sampled with the aid of a common post-processing clock of the resampling device, and digital auxiliary signals xd(nk+j) and yd(nk+j) are formed in the process by the insertion of zero values. In this case, the resampling device 11 is designed with regard to its post-processing clock such that the latter is at least twice as fast as the fastest operating clock during the formation of the digital input signals x(k). For example, if the sampling frequencies for obtaining the digital input signals x(k) are between approximately 1 and 40 kHz, a frequency range of between 10 and 500 kHz comes into consideration for the post-processing clock; approximately 200 kHz may be recommended.

The digital auxiliary signals xd(nk+j) and yd(nk+j) with the comparatively high post-processing clock are fed in each case to an interpolation filter 12 and 13, respectively, which is an integrator in each case in the exemplary embodiment illustrated. The integrators are used in each case because differentiators have been used as signal encoders 3. A transmission characteristic with the value 1 thereby results with regard to the mode of operation of the signal encoder 3 and of the integrator 12 of the signal decoder 10.

Page 7, please replace the paragraph beginning on line 5 with the following rewritten paragraph:

The pulse trains x(nk+j) and y(nk+j) formed at the output of the integrators 12 and 13 are synchronized and are respectively fed to an anti-aliasing filter 14 and 15, by means of which filters the pulse trains are limited to the bandwidth required for processing in an evaluation device (not illustrated). The result is the reduction of digital output signals x(m) at the output of one anti-aliasing filter 14, and y(m) at the output of the other anti-aliasing filter 15. These digital output signals x(m) and y(m) can now be reduced in a known way to a sampling rate which is suitable for an evaluation device (not illustrated). This sampling rate produced by means of an integral devisor from the sampling rate of the resampling device 11. For the assumed frequencies, reasonable values are between about 0.6 and 10 kHz for applications in the monitoring of electric power supply systems.

Page 7, please replace the paragraph beginning on line 32 with the following rewritten paragraph:

Figure 2 illustrates an exemplary embodiment for a signal encoder 3 in accordance with Figure 1, which is designed as an FIR filter acting as a differentiator. In Figure 3, A denotes the input of the signal encoder, and B denotes the output. The digital input signal x(k) is used to form the pulse train xd(k). The coefficients $a_0$, $a_1$ and $b_1$ of the signal coder 3 are dimensioned as follows:

Page 8, please replace the paragraph beginning on line 5 with the following rewritten paragraph:

In Figure 3(a), the amplitude characteristic is illustrated plotted against the frequency of the signal encoder according to Figure 2, while in Figure 3(b) the phase characteristic is reproduced plotted against the frequency of such a filter.

Page 8, please replace the paragraph beginning on line 20 with the following rewritten paragraph:

In Figure 5(a), the amplitude characteristic is shown plotted against the frequency of the filter according to Figure 4, and Figure 5(b) the phase characteristic is shown plotted against the frequency of such a filter. It may be seen that the frequency characteristics of the filters according to Figures 2 and 4 are inverse relative to one another, and this leads to the targeted transmission function having the value 1.

Page 8, after line 28, please insert the following paragraph:

While the invention has been explained with respect to the embodiments described above, it will be apparent to those skilled in the art that various modifications and improvements may be made without departing from the spirit and scope of the invention. Accordingly, it is to be understood that the invention is not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.

**IN THE CLAIMS:**

Page 9, please replace the heading with the following rewritten heading:

WHAT IS CLAIMED IS:

Please amend the claims as follows.

1. (Amended) A method for synchronizing a plurality of digital input signals, which are formed by sampling with a dedicated operating clock in each case, comprising:

forming digital auxiliary signals by sampling the digital input signals with a common post-processing clock and a post-processing clock which is at least twice as fast as the fastest operating clock; and